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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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8021-225 (SS-18860-US)

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EXAMINER

CAMPOS, YAIMA

ART UNIT

PAPER NUMBER

2185

MAIL DATE

DELIVERY MODE

05/04/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/814,968	Applicant(s) SOHN ET AL.	
	Examiner Yaima Campos	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 February 2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-3, 5-13, 15 and 21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6, 8-13 and 15 is/are rejected.
- 7) ☒ Claim(s) 5, 7 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. The examiner acknowledges the applicant's submission of the amendment dated February 16, 2007. At this point claims 1, 12-13 and 15 have been amended, and claims 4, 14, 16-20 and 22 have been cancelled. Thus, 14 claims are pending in the instant application.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112 First Paragraph

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. **Claims 1-3, 5-13, and 15** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

4. The claim language used in claims 1 and 12 is ambiguous and contradictory as applicant recites "is performed" versus "is not performed."

Claim Rejections - 35 USC § 112 Second Paragraph

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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6. **Claims 1-3 and 5-11** are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are:

7. **Claim 1** recites “a tag memory controlling unit, which writes... when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and the read address are the same” which renders claim 1 as a conditional claim which is not limiting except when access to the sub-memory block is simultaneously performed and when the write address is the same as the read address. Claim 1 must be corrected to recite what happens when access to the sub-memory block is not simultaneous and when the write address and the read address are not the same.

8. Any claim not specifically addressed above is rejected for encompassing the deficiencies of a claim upon which it depends and for not correcting the deficiencies of a claim upon which it depends.

9. **Claims 12** is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are:

10. Claim 12 recites “determining... when the write address and the read address have been input during the period of the clock signal” and “performing... when the upper addresses of the write and read addresses are the same” which renders claim 12 as a conditional claim which is not limiting except when the write address and the read address have been input during the period of the clock signal and when the upper of the write and read addresses are the same. Claim 12 must be corrected to recite what happens when the write address and the read address

have not been input during the period of the clock signal and when the upper address of the write address and the read address are not the same.

Claim Rejections - 35 USC § 101

11. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 1-3, 5-11 and 12 are rejected under 35 U.S.C. 101 because they do not recite a practical application by producing a physical transformation or producing a useful, concrete, and tangible results. To perform a physical transformation, the claimed invention must transform an article of physical object into a different state or thing. Transformation of data is not a physical transformation. A useful, concrete, and tangible results must be either specifically recited in the claim or flow inherently therefrom. To be useful the claimed invention must establish a specific, substantial, and credible utility. To be concrete the claimed invention must be able to produce reproducible results. To be tangible the claimed invention must produce a practical application or real world result.

13. **Claim 1** recites “a tag memory controlling unit, which writes... when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and the read address are the same;” therefore, claim 1 fails to provide a concrete and tangible result when access to the sub-memory block is NOT simultaneously performed and when the write address is NOT the same as the read address.

14. Any claim not specifically addressed above is rejected for encompassing the deficiencies of a claim upon which it depends and for not correcting the deficiencies of a claim upon which it depends.

15. Claim 12 recites “determining... when the write address and the read address have been input during the period of the clock signal” and “performing... when the upper addresses of the write and read addresses are the same;” therefore, Claim 12 fails to produce a concrete and tangible result when the write address and the read address have not been input during the period of the clock signal and when the upper address of the write address and the read address are not the same.

REJECTIONS BASED ON PRIOR ART

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. **Claims 1 and 12** are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 14 and 18 respectively of copending Applications No. 10/811,613.

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2. Initially, it should be noted that the present application and Application No. 10/811,613, have the same inventive entity. The assignee for both applications is Samsung Electronics Co., Ltd.

3. Claimed subject matter in the instant application is fully disclosed in the referenced copending application and would be covered by any patent granted on that copending application since the referenced copending application and the instant application are claiming common subject matter, as noted below. *See In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993).*

4. Furthermore, there is no apparent reason why applicant would be prevented from presenting claims corresponding to those of the instant application in the other copending application. See MPEP § 804.

16. **Claim 1 and 12** are rejected on the ground of nonstatutory double patenting over claims 32, 22, and of U. S. Patent No. 6,826,088 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

See claim 1 in the instant application compared to claim 32 of U.S. Patent No. 6,826,088 and Claim 12 of the instant application compared to claim 22 of U.S. Patent No. 6,826,088.

Furthermore, there is no apparent reason why applicant was prevented from presenting claims corresponding to those of the instant application during prosecution of the application

which matured into a patent. See *In re Schneller*, 397 F.2d 350, 158 USPQ 210 (CCPA 1968).

See also MPEP § 804.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. **Claims 1-3, 8-13 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu (US 5,752,260) in view of Favor (US 6,141,742).

19. As per **claim 1**, Liu discloses

An integrated circuit to which inputs and outputs (I/Os) are separately provided and to which a write address and a read address are simultaneously input during one period of a clock signal, the integrated circuit comprising: as [**“memory 10” and explains “the memory 10 is capable of being simultaneously accessed by multiple ports for access in the same cycle” (Figure 1; Col. 3, line 58-Col. 4, line 3)**]

“a plurality of memory blocks, each of the memory blocks comprising a plurality of sub-memory blocks;” [**“cache memory device 10 having multiple subarrays” (Col. 3, lines 5-33) and explains “the features of the present invention may be useful in various systems, as primary (first level cache), secondary cache, translation buffers, and the like, wherever a content-addressable memory is useful, or wherever multiple access, multiple-port memory is needed” (Col. 6, line 62-Col. 7, line 2). Therefore, a single system may contain multiple memories such as “memory 10” which are divided into multiple sub-arrays]**

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“a plurality of data memory blocks corresponding to the memory blocks, wherein each of the data memory blocks has the same size as a sub-memory block;” [With respect to this limitation, Liu discloses “main memory 115” and explains “the main memory 115 usually contains a subset of what is in the disk storage 116, the secondary cache 110 contains a subset of what is in the main memory 115, and the on-chip caches 10 and 109 subsets of what is in the secondary cache” (Figure 6; Col. 7, lines 1-50)]

“and a tag memory controlling unit, which writes data to the memory blocks or reads data from the memory blocks in response to the write address or the read address, wherein access to the same sub-memory block is not simultaneously performed when the write address and the read address are the same” [With respect to this limitation, Liu discloses “arbitration/priority circuit 80” and explains “if subarray select fields of any two addresses contain the same value, then these two addresses have a subarray conflict and some predefined priority is used to allow the higher priority one to access the subarray... the constraint that one subarray can be accessed by only one address is due to the fact that there can be only one word line enabled in one subarray in any one cycle” (Col. 2, lines 17-46; Col. 4, lines 4-27; Col. 5, line 52-Col. 6, line 32; Figure 1; Figure 6)].

Liu does not disclose expressly “wherein a write operation or a read operation is performed in a data memory block and one of the write operation and the read operation not performed in the data memory block is performed in a sub-memory block when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and read address are the same.”

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Favor discloses “wherein a write operation or a read operation is performed in a data memory block and one of the write operation and the read operation not performed in the data memory block is performed in a sub-memory block when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and read address are the same” as [“**the load unit 240 and the store unit 242 respectively load (read) data or store (write) data to the data cache 216 (L1 data cache), the L2 cache 122 and the main memory 130 while executing a load/storage operation (LdStOp). A store queue 262 temporarily stores data from store unit 242 so that store unit 242 and load unit 240 operate in parallel without conflicting accesses to data cache 216**” (Col. 6, lines 52-67; Figure 2 and related text)].

Liu (US 5,752,260) and Favor (US 6,141,742) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory access system as taught by Liu and further “wherein a write operation or a read operation is performed in a data memory block and one of the write operation and the read operation not performed in the data memory block is performed in a sub-memory block when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and read address are the same” as taught by Favor.

The motivation for doing so would have been because Favor discloses [A store queue 262 temporarily stores data from store unit 242 so that store unit 242 and load unit 240

operate in parallel without conflicting accesses to data cache 216” (Col. 6, lines 52-67;

Figure 2 and related text)

Therefore, it would have been obvious to combine Liu (US 5,752,260) with Favor (US 6,141,742) for the benefit of creating an integrated circuit to obtain the invention as specified in claim 1.

20. As per **claim 2**, the combination of Liu and Favor discloses the integrated circuit of claim 1, [See rejection to claim 1 above] wherein “the sub-memory blocks are a set of memory cells for sharing a common word line or bit line” [(Col. 2, lines 24-46; Col. 5, line 52-Col. 6, line 32)].

21. As per **claim 3**, the combination of Liu and Favor discloses the integrated circuit of claim 1, [See rejection to claim 1 above] wherein “in the sub-memory blocks, two or more word lines or bit lines cannot be simultaneously activated” [(Col. 2, lines 24-46; Col. 5, line 52-Col. 6, line 32)].

22. As per **claim 8**, the combination of Liu and Favor discloses the integrated circuit of claim 1, [See rejection to claim 1 above] wherein “the tag memory controlling unit stores a data memory address indicating that data stored in the data memory blocks is originally data corresponding to one of the sub-memory blocks, and validity determination information for determining whether data stored in the data memory block is valid” [Liu discloses this concept as “MESI status bits” (Col. 3, lines 33-45; Col. 4, lines 4-27)].

23. As per **claim 9**, the combination of Liu and Favor discloses the integrated circuit of claim 8, [See rejection to claim 8 above] wherein “if the number of the sub-memory blocks is $2N$, each address of the tag memory controlling unit includes $N+1$ data bits, and N -bit of the $N+1$

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data bits indicates a data memory address, and remaining 1-bit of the N+1 data bits indicates the validity determination information” [Liu discloses this concept as “MESI status bits” (Col. 3, lines 33-45; Col. 4, lines 4-27)].

24. As per claim 10, the combination of Liu and Favor discloses the integrated circuit of claim 1, [See rejection to claim 1 above] wherein “the data memory blocks have a direct mapping relation with the sub-memory blocks” [“the main memory 115 usually contains a subset of what is in the disk storage 116, the secondary cache 110 contains a subset of what is in the main memory 115, and the on-chip caches 10 and 109 subsets of what is in the secondary cache” (Col. 7, lines 1-50; Figure 6)].

25. As per claim 11, the combination of Liu and Favor discloses the integrated circuit of claim 1, [See rejection to claim 1 above] wherein “the data is input or output at a single data rate (SDR) or a double data rate (DDR)” [“the memory 10 is a static RAM device” (Col. 3, lines 5-33; Figure 5)].

26. As per claims 12-13 and 15, Liu discloses “a method for simultaneously performing a write operation and a read operation in an integrated circuit comprising a separate input and output, the method comprising:” [“memory 10” and explains “the memory 10 is capable of being simultaneously accessed by multiple ports for access in the same cycle” (Figure 1; Col. 3, line 58-Col. 4, line 3)] “determining if a write address and a read address have been input during a period of a clock signal;” [“the memory 10 may receive two 64-bit EA (effective) addresses EA0 and EA1 on lines 24 and 25, and one 40-bit (real) address on lines 26, at the same time. The memory...

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decides which two addresses are used to produce output data” (Col. 3, line 58-Col. 4, line 3)]

“determining if an upper address of the write address is the same as an upper address of the read address when the write address and the read address have been input during the period of the clock signal;” **[“if subarray select fields of any two addresses contain the same value, then these two addresses have a subarray conflict and some predefined priority is used to allow the higher priority one to access the subarray” (Col. 2, lines 24-46; Col. 4, lines 4-51; Col. 5, line 52-Col. 6, line 32; Figures 1-4)]**

“and performing a write operation and a read operation during the period of the clock signal when the upper addresses of the write and read addresses are the same or when the upper addresses of the write and read addresses are not the same” **[With respect to this limitation, Liu discloses “the constraint that one subarray can be accessed by only one address is due to the fact that there can be only one word line enabled in one subarray in any one cycle. If these three address contain different values in the subarray select field, then three different operations can happen in the same cycle at three different subarrays. For example, while a ECAM read on behalf of the EA0 address is accessing the subarray 0, another ECAM read on behalf of an EA1 address may be accessing subarray 1, and a store cycle on behalf of a real address RA is accessing subarray 2” (Col. 2, lines 24-46)].**

Liu does not disclose expressly “performing a write operation or a read operation in a data memory block and performing on of the write operation an the read operation not performed in the data memory block in a sub-memory block during one period of the clock signal when the upper addresses of the write and read addresses are the same.”

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Favor does not disclose expressly “performing a write operation or a read operation in a data memory block and performing on of the write operation an the read operation not performed in the data memory block in a sub-memory block during one period of the clock signal when the upper addresses of the write and read addresses are the same.”

[“the load unit 240 and the store unit 242 respectively load (read) data or store (write) data to the data cache 216 (L1 data cache), the L2 cache 122 and the main memory 130 while executing a load/storage operation (LdStOp). A store queue 262 temporarily stores data from store unit 242 so that store unit 242 and load unit 240 operate in parallel without conflicting accesses to data cache 216” (Col. 6, lines 52-67; Figure 2 and related text)].

Liu (US 5,752,260) and Favor (US 6,141,742) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory access system as taught by Liu and further “wherein a write operation or a read operation is performed in a data memory block and one of the write operation and the read operation not performed in the data memory block is performed in a sub-memory block when access to the sub-memory block and corresponding data memory block is simultaneously performed when the write address and read address are the same” as taught by Favor.

The motivation for doing so would have been because Favor discloses **[A store queue 262 temporarily stores data from store unit 242 so that store unit 242 and load unit 240 operate in parallel without conflicting accesses to data cache 216” (Col. 6, lines 52-67; Figure 2 and related text)**

Therefore, it would have been obvious to combine Liu (US 5,752,260) with Favor (US 6,141,742) for the benefit of creating an integrated circuit to obtain the invention as specified in claim 12-13 and 15.

27. **Claim 6** is rejected under 35 U.S.C. 103(a) as being anticipated by Liu (US 5,752,260) in view of Favor; and further in view of Arimilli et al. (US 2003/0097529).

28. As per **claim 6**, the combination of Liu and Favor discloses the integrated circuit of claim 1, [See rejection to claim 1 above] wherein but does not discloses “the tag memory controlling unit has a same number of decoding addresses as a number of addresses for decoding the data memory blocks;” however, it is the examiner’s position that this feature is well known in the art as evidenced by [(Arimilli, Figure 4; Page 8, Par. 0090-Page 9, Par. 0094) wherein, it is taught having a cache memory and a tag storage including the same number of entries as that the tag memory; therefore, there must be one tag for every entry in the cache].

CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

29. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i):

a(1) SUBJECT MATTER CONSIDERED ALLOWABLE

30. Per the instant office action, **5, 7 and 21** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

a(2) CLAIMS REJECTED IN THE APPLICATION

31. Per the instant office action, claims 1-3, 6, 8-13 and 15 have received a second action on the merits and are subject of a second action non-final.

a(3) CLAIMS NO LONGER IN THE APPLICATION

32. Claims 4, 14, 16-20 and 22 was cancelled by the amendment dated February 16, 2007.

b. DIRECTION OF FUTURE CORRESPONDENCES

33. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

34. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions

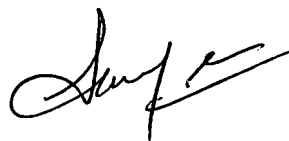
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on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Yaima Campos
Examiner
Art Unit 2185

April 27, 2007



SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100